Teaching Research Methodology Based on Research Results: an Experience Sharing

by Assoc. Prof. Emilie Avignon-Meseldzija, PhD, CentraleSupélec, UPS, France

30th June 2025

Erasmus+ Cooperation partnerships in higher education (KA220-HED)

Project CONN'COR
2024-1-FR01-KA220-HED-000250882

WP3: R3.4a Teachers trained for Research-Based Teaching

Outline

1. Context and Organization
2. Preparation steps
3. Evaluation of the work
4. Valorization and networking
5. Results of students survey
6. Conclusion

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Outline

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1. **Context and Organization**
   - **The ICS Master at Université Paris Saclay**
   - **The Students background**
   - **The teachers**
   - **Organization**
2. Preparation steps
3. Evaluation of the work
4. Valorization and networking
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The ICS Master at Université Paris Saclay

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https://www.universite-paris-saclay.fr/en/education/master/electrical-engineering/m2-integration-circuits-systems#presentation

The objective of the M2 "Integration Circuits and Systems" is to train future researchers or engineers with extensive knowledge and skills in advanced domains of electronic design:

- hyper-frequencies,
- components and systems for telecommunications,
- decananometric microelectronics,
- microsystems (MEMS/NEMS),
- analogic and digital embedded systems,
- Analog-to-Digital conversion, etc.

This M2 is based on courses given by 3 establishments considered as references in this domain: CentraleSupélec, Télécom ParisTech and Paris-Sud University.

Principle job opportunities: Research, R&D in electronics.

The students background

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ICS Master students are mostly international students (Brazil, Viet-Nam, China, Iran, Pakistan, Lebanon, Egypt, India, England, etc…).

Some of the ICS Master students are Master-level students from CentraleSupélec wanting to deepen their skills in the electronics domain.

All these students have a strong electronics backgroung and always want to know more. They are attracted by Industry but numerous students would like to pursue with a PhD.

This academic year, there were 24 ICS Master students.

The teachers

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Viet Nguyen-Thien graduated from Hanoi University of Science and Technology (HUST), Vietnam, in 2021, and received the M.Sc. degree in electronics from Télécom Paris, France, in 2023, where he is currently pursuing the Ph.D. degree.

Viet was also a student from the same ICS Master and graduated in 2023. He understands expectations of ICS Master students.

Viet, in accordance with his supervisors, accepted to share his PhD topic with current ICS Master.

…….

Emilie Avignon-Meseldzija graduated the Ph.D. degree from the Pierre et Marie Curie University (currently Sorbonne University), Paris, France, in 2007. Since then, she joined the GeePs Laboratory as an Associate Professor with the Department of Electronics and Electromagnestism of CentraleSupélec, Université Paris-Saclay.

I taught for many years in the ICS Master and I am responsible of the courses “Architecture of Analog Circuits” and “Computer Aided Design of Analog Integrated Circuits”.

Organization (1)

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The little story of this « Research based teaching »:

An Assoc. professor resigned from CS to become professor in another University

I was asked for a replacement of 24 hours of labworks session in the ICS Master. Topic was RF Layout.

I asked the head of the Master if I could use these 24 hours for this « Research-Based Teaching » experience to include it in Erasmus+ CONN'COR project.

Permission was granted and the experience was held from mid-February to the end of March.

Organization (2)

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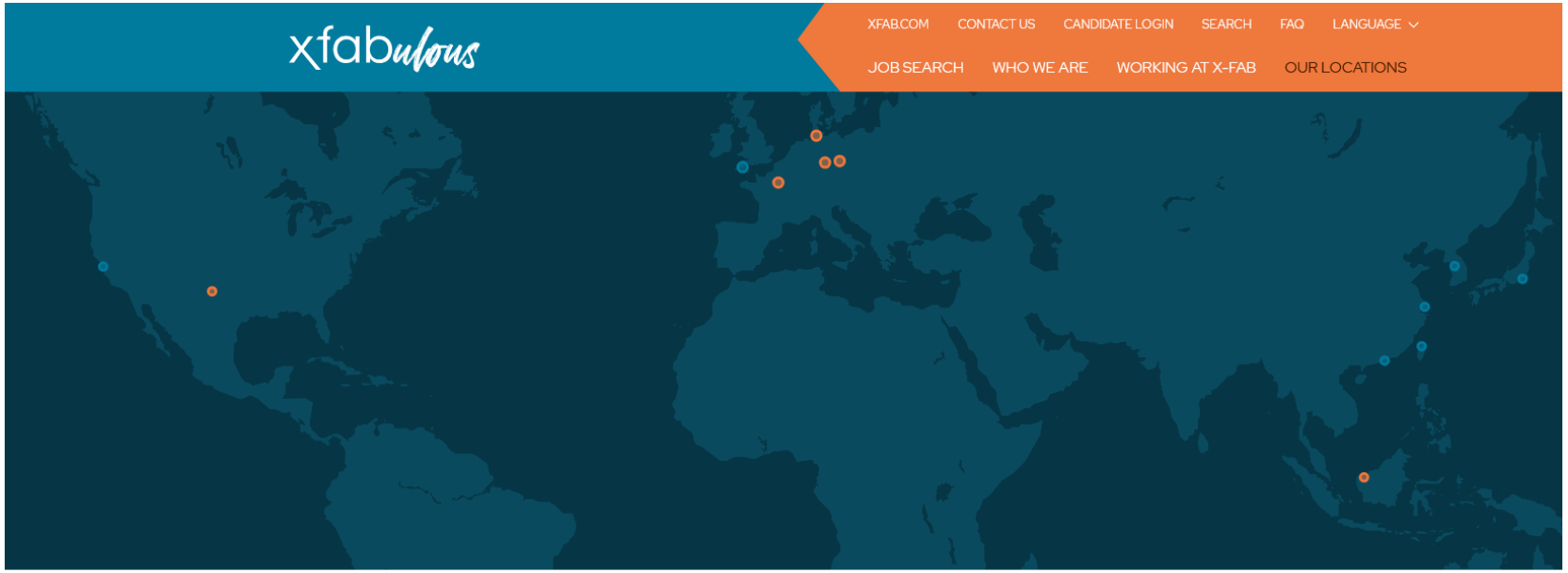
Introduction to the course: Two seminars from XFAB

XFAB an important industrial actor in micro/nanoelectronics



OUR LOCATIONS

Our more than **4,500 employees** are based all over the globe – with **six manufacturing sites** on **three continents**, it is quite

Integrated Electronics Manufacturing: From the physics of semiconductors to the economy of integrated electronics through modern industrial integration processes (12th of February 2025)

Modeling, Characterization, and Simulation for Modern Industrial Technologies (24th of February 2025)

Organization (3)

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24h of labwork/project:

3h00 (Wed. 5th of March 2025 8:30AM): introduction and choice of the subject
3h00 (Wed. 12th of March 2025 8:30AM)
4h30 (Thur. 13th of March 2025 1:30 PM)
3h00 (Wed. 19th of March 2025 8:30AM)
4h30 (Thur. 20th of March 2025 1:30 PM)
3h00 (Wed. 19th of March 2025 8:30AM)
3h00 (Thur. 27th of March 2025 1:30 PM) :

- **The 24 students work in a labroom on with XFAB technology design kit with industry compatible Cadence Virtuoso Software**
- **They are invited to work more than these 24 hours…**
- **They work by pair, so 12 subjects are needed**

Outline

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1. Context and Organization
2. **Preparation steps**
   - **Creating the subjects**
   - **Selecting a reduced bibliography**
   - **Defining specific content**
   - **Creating specific tutorials**
   - **Specific support**
3. Evaluation of the work
4. Valorization and networking
5. Results of students survey
6. Conclusion

Creating the subjects

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- **24 students working by pair**

- **12 projects needed**

Meetings between the teachers to define the projects in link with our research.

7 research topics have been identified:

1. Ultra low-power capacitance multiplier (2 pairs + 1 student),
2. Ultra low-power squarer (1 pair + 1 student),
3. High output impedance current frequency synthesizer (not selected),
4. Towards a complex dispersive analog filter (2 pairs + 1 student),
5. High-performance transimpedance amplifier (2 pairs),
6. Variable gain amplifier (VGA) (2 pairs),
7. High-performance comparator (1 pair),

Selecting a reduced bibliography

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The experience is limited in time (1 month 24h00 in the labroom)

We had to read numerous articles to:

- **Preselect the most pedagogical ones for each topic**
- **Preselect the ones with the highest possibility of achievement in a reduced time**
- **To insure 2 or 3 versions of one topic to reach 12 subjects**

This step took days of preparation for both teachers

Defining specific content

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What knowledge/sills do they have?

Classical Architecture of Analog Circuits

Design and simulation of a system at transistor, evaluation of performances,
Sizing of transistors, Improvement of the sizing

Layout drawing

DRC (Design Rule Check)

LVS (Layout Versus Schematic)

Extraction of parasitic resistances and capacitances, evaluation of performances

What novel skills could they learn?

- A deeper vision of an integrated circuits research domain: communication, biomedical applications, MEMS instrumentation…
- Specific design techniques
  - Low noise design
  - Ultra low power design: design in subthreshold
  - RF design
- New circuits architectures (translinear loop, mitigation loop…)
- Advanced Cadence: noise, worst case, Monte-Carlo simulation

Creating specific tutorials

by Viet Nguyen-Thien

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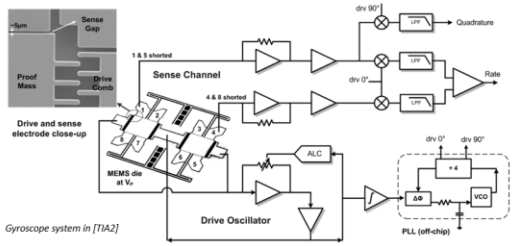
Drive interface circuit for MEMS gyroscope

Sensor parameters:

- Bias frequency $f_{bias} = 50\ kHz$, bandwidth $BW = 1\ kHz$
- Maximum current amplitude $100\ nA$, in-band current density $1\ pA/\sqrt{Hz}$
- Parasitic capacitance at drive output $C_p = 50\ pF$



Gyroscope system in [TIA2]

Resistor noise

Resistor thermal noise:
The thermal noise of a resistor R can be modeled by a **series voltage** source with the spectral density of

$$v_n^2 = 4kTR,$$

or by a **parallel current** source

$$i_n^2 = \frac{4kT}{R},$$

where $k = 1.38 \times 10^{-23} J/K, T = 300\ °K$.

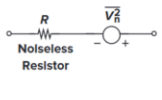
Note that v_n^2 and i_n^2 are expressed in V^2/Hz and A^2/Hz, respectively.

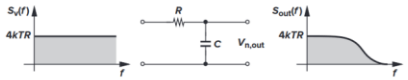
kT/C noise:
Noise spectrum shaping by a RC low-pass filter:

$$v_{n,out}^2 = 4kTR \times \frac{1}{1 + R^2C^2\omega^2}$$

The total noise power at the output:

$$P_{n,out} = \int_0^{\infty} \frac{4kTR}{1 + 4\pi^2R^2C^2f^2} df = \frac{kT}{C}$$





Ref:
B. Razavi, Design of Analog CMOS Integrated Circuits - Razavi. 2016.

MOSFET noise

The MOSFET noise is dominated by thermal and flicker (1/f) noises:
The MOSFET noise can be modeled by a **drain current** with the spectral density of

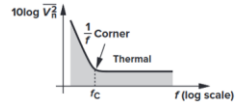
$$i_n^2 = \frac{8kTg_m}{3} + \frac{I_D C_1}{fL^2},$$

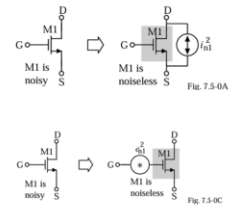
or by a **gate voltage**

$$v_n^2 = \frac{8kT}{3g_m} + \frac{C_2}{fWL},$$

where $k = 1.38 \times 10^{-23} J/K, T = 300\ °K$, C_1 and C_2 are process-dependent constants. Note that v_n^2 and i_n^2 are expressed in V^2/Hz and A^2/Hz, respectively.

Other MOSFET noise: shot noise (in subthreshold), gate resistor noise





Ref:
P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design.
B. Razavi, Design of Analog CMOS Integrated Circuits - Razavi. 2016.

Noise analysis example

TIA

- Feedback resistor noise $i_{n,R_f}^2 = \frac{4kT}{R_f}$ (thermal)
- Opamp input voltage noise $v_{n,opamp}^2$ (thermal + flicker) is equivalent to a current noise of

$$i_{n,opamp}^2 = \frac{v_{n,opamp}^2}{\left[R_f // \frac{1}{\omega_{bias}(C_p // C_f)}\right]^2} = v_{n,opamp}^2 \left[\frac{1}{R_f} + (C_p // C_f)\omega_{bias}\right]^2$$

- The TIA total input-referred current noise is then

$$i_{n,TIA}^2 = i_{n,R_f}^2 + i_{n,opamp}^2$$

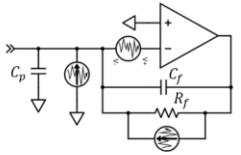


Figure from Prof. Jérôme Juillard's slides.

Noise analysis example

Inverting amplifier

- Equivalent resistor noise at the opamp input $v_{n,R}^2 = 4kT(R_{in} // R_f)$
- Opamp input voltage noise $v_{n,opamp}^2$ (thermal + flicker)
- The total input-referred voltage noise is then

$$v_{n,InvAmp}^2 = (v_{n,R}^2 + v_{n,opamp}^2) \times \left(\frac{R_f + R_{in}}{Rf}\right)^2$$

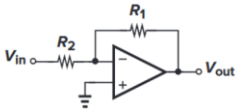


Figure from:
B. Razavi, Design of Analog CMOS Integrated Circuits - Razavi. 2016.

Two-stage CMOS Operational Amplifier (OpAmp)

Design procedure

This is a simplified design procedure. Optimization is recommended after.
For best performance, keep all transistors in saturation.
Start with $L_i = L = 0.5\ \mu m$ for all transistors.

1. Estimate $g_{m1,2}$ based on noise requirement: The input pair (M1,2) contributes most of the opamp input noise, a good approximation would be $v_{n,opamp}^2 \approx 4 \times v_{n1,2}^2 = 4 \times \frac{8kT}{3g_{m1,2}}$.
2. Choose $C_c > 0.22C_L$ (C_L includes load and feedback capacitances). Then, g_{m6} should be $2.2g_{m1,2}(C_L/C_c)$.
3. Assuming $(g_m/I_D)_i = 15$, calculate g_{mi} and I_{Di}.
4. With $\frac{W_i}{L_i} = \frac{(g_m/I_D)_i^2}{2K_t} \times I_{Di}$, where $K_n = 240\mu A/V^2, K_p = 70\mu A/V^2$, calculate W_i.
5. Simulate and refine W_i and L if needed.

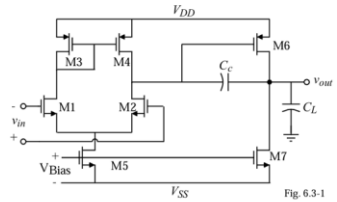


Fig. 6.3-1

Ref:
P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design.
Course notes: 2016 Short Course Notes – AICDESIGN.ORG

Creating specific tutorials

by Emilie Avignon-Meseldzija

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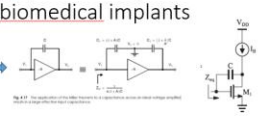
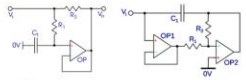
1. Ultra-low power capacitance multiplier dedicated to biomedical implants

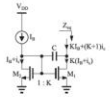
Technique 1: Miller effect



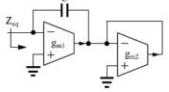
Technique 2: Opamp based



Technique 3: Current mode



Technique 4: Gm-C

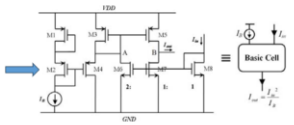


/!\ Objective /!\
- Get the largest capacitance
- Get the smallest possible real part

2. Ultra-low power squarer dedicated to biomedical monitoring implants

2nd solution: Translinear Multipliers
based on « **Translinear Loop** »

Unusual!

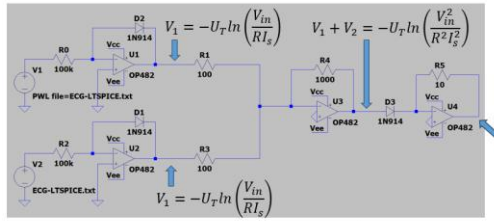


A. N. Saatlo, S. Ozoguz and S. Minaei, "Applications of a CMOS current squaring circuit in analog signal processing," *2015 38th International Conference on Telecommunications and Signal Processing (TSP)*, Prague, Czech Republic, 2015, pp. 339-343, doi: 10.1109/TSP.2015.7296280.

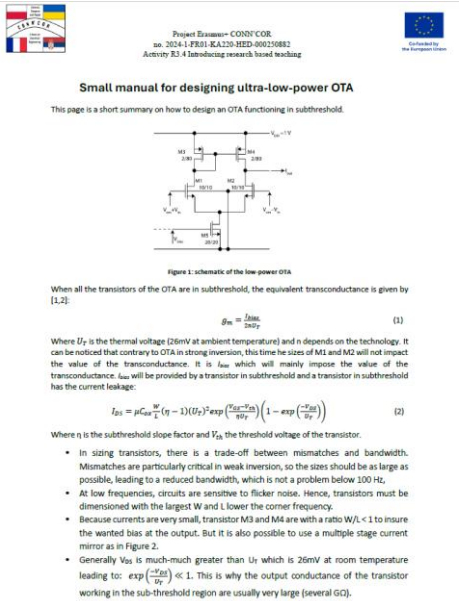
J. M. A. Algueta Miguel, C. A. De La Cruz Blas and A. J. Lopez-Martin, "Fully Differential Current-Mode CMOS Triode Translinear Multiplier," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 1, pp. 21-25, Jan. 2011, doi: 10.1109/TCSII.2010.2092821

2. Ultra-low power squarer dedicated to biomedical monitoring implants

1st solution: inspired from diode/Opamp discrete component architecture



Design steps:
In PRIMLIB library: Different diodes to test
Design of ultra low power Opamp
Pseudo-resistors



Project Erasmus+ CONN'COR
no. 2024-1-FR01-KA220-HED-000250882
Activity R3.4 Introducing research based teaching

Small manual for designing ultra-low-power OTA

This page is a short summary on how to design an OTA functioning in subthreshold.

Figure 1: schematic of the low-power OTA

When all the transistors of the OTA are in subthreshold, the equivalent transconductance is given by [1,2]:

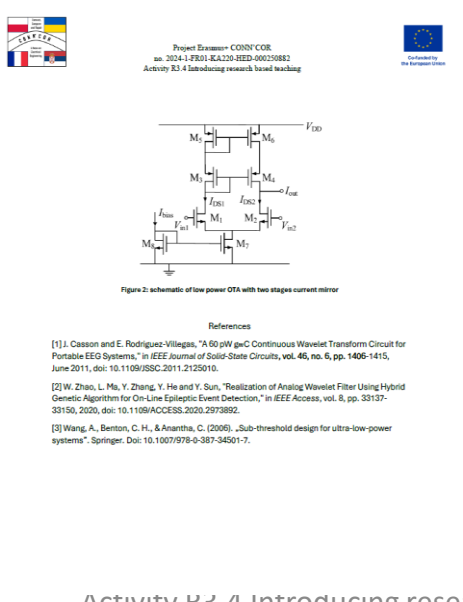
$$g_m = \frac{I_{bias}}{2nU_T} \quad (1)$$

Where U_T is the thermal voltage (26mV at ambient temperature) and n depends on the technology. It can be noticed that contrary to OTA in strong inversion, this time he sizes of M1 and M2 will not impact the value of the transconductance. It is I_{bias} which will mainly impose the value of the transconductance. I_{bias} will be provided by a transistor in subthreshold and a transistor in subthreshold has the current leakage:

$$I_{DS} = \mu C_{ox} \frac{W}{L} (\eta - 1)(U_T)^2 exp\left(\frac{V_{GS} - V_{th}}{\eta U_T}\right)\left(1 - exp\left(\frac{-V_{DS}}{U_T}\right)\right) \quad (2)$$

Where η is the subthreshold slope factor and V_{th} the threshold voltage of the transistor.

- In sizing transistors, there is a trade-off between mismatches and bandwidth. Mismatches are particularly critical in weak inversion, so the sizes should be as large as possible, leading to a reduced bandwidth, which is not a problem below 100 Hz,
- At low frequencies, circuits are sensitive to flicker noise. Hence, transistors must be dimensioned with the largest W and L lower the corner frequency.
- Because currents are very small, transistor M3 and M4 are with a ratio W/L < 1 to insure the wanted bias at the output. But it is also possible to use a multiple stage current mirror as in Figure 2.
- Generally V_{DS} is much-much greater than U_T which is 26mV at room temperature leading to: $exp\left(\frac{-V_{DS}}{U_T}\right) \ll 1$. This is why the output conductance of the transistor working in the sub-threshold region are usually very large (several GΩ).



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no. 2024-1-FR01-KA220-HED-000250882
Activity R3.4 Introducing research based teaching

Figure 2: schematic of low power OTA with two stages current mirror

References

[1] J. Casson and E. Rodriguez-Villegas, "A 60 pW gmC Continuous Wavelet Transform Circuit for Portable EEG Systems," in *IEEE Journal of Solid-State Circuits*, **vol. 46, no. 6, pp. 1406**-1415, June 2011, doi: 10.1109/JSSC.2011.2125010.

[2] W. Zhao, L. Ma, Y. Zhang, Y. He and Y. Sun, "Realization of Analog Wavelet Filter Using Hybrid Genetic Algorithm for On-Line Epileptic Event Detection," in *IEEE Access*, vol. 8, pp. 33137-33150, 2020, doi: 10.1109/ACCESS.2020.2973892.

[3] Wang, A., Benton, C. H., & Anantha, C. (2006). „Sub-threshold design for ultra-low-power systems". Springer. Doi: 10.1007/978-0-387-34501-7.

+ a video tutorial about Cadence/Virtuoso Monte-Carlo simulation

Specific support

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Some students, even motivated, needed strong support

At the end of a project session, check if any students are blocked

Between two sessions:
- **Think about their problems**
- **Investigate to propose a solution/explanation: a model, a simulation, an article**

At the beginning of the next session, discuss with the students and propose solutions

Big difference with a classical teaching, where all students have the same subject with available correction

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Evaluation of the work (1)

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- Research Results cannot be evaluated only after a couple of labwork/project sessions but Research Methodology yes.

- Evaluation will be based on:
  - An IEEE-type two column article
  - Initiative from the students all along the sessions to solve the problems

- What can be evaluated is:
  - Subject understanding
  - Do the students succeed to explain the trade-off and difficulties of their design
  - Do the students take initiative to find solutions, or do they wait for external help?
  - Are the students capable of presenting their subject with clarity in 10 minutes to a non-informed audience?

Evaluation of the work (2)

	High-performance transimpedance amplifier (TIA) for MEMS sensors		Variable-Gain Amplifier (VGA)		Comparator
Circuit design (10/20)	**7**	**9**	**6**	**9**	**9**
Comprehend the context and trade-off of the proposed research topic	2	2	2	2	2
Understand the selected article	2	2	2	2	2
How autonomous the students were	1 - The students only mentioned technical problems when asked.	2	0. The students really started to work on the design during the few last sessions.	2	2
Did the students keep motivation to go as far as possible (layout, worst-case, Monte-Carlo)?	0 - Only minimum-required simulation with the schematic was carried out.	2 - Layout and worst-case simulation were carried out.	0 - Only pre-layout simulation was carried out. The layout is incomplete.	1 - Full layout with the biasing and control circuits. No worst-case simulation.	2 - Layout and offset Monte-Carlo simulation were completed.
Did they apply efficiently what they learnt before or the provided materials (sizing, layout...)?	2	1 - Some of the design choices were not fully clarified, for example, the selections of feedback resistance and OTA bias current.	2	2	1 - The bias current was selected without considering noise.
Two-column article (10/20)	**5**	**7**	**7**	**8**	**7**
Is the article well written (layout, clarity, coherence...)?	2	1 - The students focused too much on listing the design eqution but not the arguments for the design choices.	1 - The sub-sections II.B.3 is redundant. Fig. 1 lacks caption, while Fig .3 and Fig.4 showed the OTA design twice...	2	2
Is the context of the research well described?	2	1 - The contexts of the MEMS system and the transimpedance amplifier were poorly mentioned in the introduction section.	2	2	1 - The advantages of hysteresis comparator were not highlighted.
Are there some mandatory references for the state-of-the-art?	0 - Lack of references to support the introduction and the design of choice. There is no comparison with state-of-the-art works.	1 - Only the selected article was included.	1 - Only the selected article was included.	1 - Only the selected article was included.	1 - Only the selected article was included.
Are the main results sufficient and clearly presented?	1 - The plot graphs are not really visible. The reasons for increasing the sizing 4 and 10 times compared to the calculated values have not been given clearly.	2	1 - The simulation plots on gain and noise were included but poorly presented. Regarding noise, there are lacks of noise plots in different gain configurations.	2	1 - No result on noise was reported.
On time submission?	0 - The article was submitted 2 days after deadline.	2	2	1 - submitted slightly late.	2
Overall (20/20)	**12**	**16**	**13**	**17**	**16**

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IEEE
Young Professionals of
Circuits and Systems Society

https://www.newcas2025.com/ypcas-event/

2 students good papers to be presented at YPE NEWCAS

3 Registrations paid by Erasmus+ CONN'COR funding (WP5 Dissemination activities)

Connect, Compare and Repair
CONN'COR
A focus on Electrical Engineering

Co-funded by
the European Union

YPCAS EVENT

Schedule 24th of June 2023 – 3:00pm-6:00pm

The Young Professionals Event at NEWCAS'25 aims to provide a platform for emerging researchers to showcase their work, gain valuable feedback, and engage in discussions with leading experts in the field of circuits and systems. This event is an excellent opportunity to present novel research, exchange ideas, and expand professional networks within the academic and industrial communities. The event will be twofold and will be open to all the audience of NEWCAS'25. A panel session on Sustainability and Eco-Design in Electronics will be followed by a poster time where YPCAS will present their work (three prizes will be awarded at the end of the session). CAS Society offers a cocktail, open to all, to accompany the event.

PANEL SESSION ON SUSTAINABILITY AND ECO-DESIGN IN ELECTRONICS

Schedule 24th of June 2023 – 3:00pm-4:15pm

2025 has seen major upheavals in people's apprehension of sustainable development, at all socio-economic levels. For sure, eco-scepticism is not the order of the day in educated circles, whether academic or industrial, but the application of sustainability-related constraints to the industrial process is still a constant endeavour that discourages many people. The dilemma is acute. In a tense political context, how can we continue our efforts in electronics and microelectronics? How do we begin a virtuous process? In spite of everything, global warming is taking its toll, on biodiversity in general, but also on our infrastructures. The global price is high, and it has to be paid by everyone. From a more pragmatic point of view, laziness in action is undermining the attractiveness of microelectronics to young people and this remains a problem in times of economic boom and recruitment. The aim of this panel is therefore to open up the discussion on sustainability issues, to present industrial initiatives in electronics that are moving in the direction of eco-design and sustainable development, and to highlight the actors of change.

INVITED SPEAKERS

- **Jean-Pierre Raskin**, PhD, Professor at Louvain School of Engineering, Belgium
- **Jean-Brieux Féron**, PhD, Founder & CEO of Citronics, Belgium
- **Thomas Delatour**, PhD, Engineer at the Service de Sobriété Numérique of ADEME, France
- **Laura Vauche**, PhD, Engineer at CEA-LETI
- **Olivier Bouchet**, MSc-MBA, Project Manager at Orange

POSTER SESSION WITH COCKTAIL

Schedule 24th of June 2023 – 4:30pm-6:00pm

A Variable Gain Amplifier for MEMS Front End

Zuo LIU[1], Longfei WANG[2], Viet Nguyen-Thien[3]
[1] ICS Master students, Université Paris-Saclay, Paris, France
[2] ICS Master students, Institut Polytechnique de Paris, Paris, France
[3] Laboratoire Traitement et Communication de l'Information, Telecom-Paris, Paris, France

***Abstract*—In this work, an analog-controlled Variable Gain Amplifier based on differential structure is proposed for the MEMS gyroscope sensor, with an input voltage of 50 to 100 mV and a target output voltage of roughly 500 mV. This design features optimization for the large voltage swing and specified gain variations, demonstrating a 360uW power consumption with simulation in XFAB xh180 technology.**

I. Introduction

In MEMS analog front-ends, a Variable Gain Amplifier (VGA) is often employed to stabilize the output of a Transimpedance Amplifier (TIA). This work proposes a VGA that amplifies the TIA output voltage from a range of 50mV to 100mV up to 500mV. The proposed design is adapted from [1] and optimized for the relatively large voltage swing and the specified gain variation.

II. Proposed Architecture

A. Principle of architecture

The proposed architecture is based on a differential amplifier, whose output voltage can by adjusted by the ratio of two bias currents IC2/IC1, which are ultimately controlled by the control voltage Vc [1], as shown in Figure 1. With $K = K_n = \frac{1}{2}(\frac{W}{L})_{M1} \cdot \mu_n C_{ox} = K_p = \frac{1}{2}(\frac{W}{L})_{M2} \cdot \mu_p C_{ox}$, and $V_{DD} = -V_{SS} = 0.9V$, the gain can be expressed as

$$A_V = \frac{g_m in}{g_m load} = \sqrt{\frac{(W/L)_{input} I_{C2}}{(W/L)_{load} I_{C1}}}$$

$$= \sqrt{\frac{(W/L)_{input}}{(W/L)_{load}} \cdot \frac{\frac{I_0}{K(V_{DD}-|V_{TH}|)^2} + (1 + \frac{V_C}{V_{DD}-|V_{TH}|})^2}{\frac{I_0}{K(V_{DD}-|V_{TH}|)^2} + (1 - \frac{V_C}{V_{DD}-|V_{TH}|})^2}} \quad (1)$$

$g_m in$ and $g_m load$ are the transconductances of $M_{17,20}$ and $M_{18,19}$ respectively. The equation (1) can be rewritten as

$$A_V(V_c) = \sqrt{\frac{(W/L)_{input}}{(W/L)_{load}}} \cdot \sqrt{\frac{k + (1 + a \cdot V_c)^2}{k + (1 - a \cdot V_c)^2}} \quad (2)$$

, where $k = \frac{I_0}{K(V_{DD}-|V_{TH}|)^2}$, and $a = \frac{1}{V_{DD}-|V_{TH}|}$.

Equation(2) exhibits decibel linear property for $k <= 1$ [1]. The gain variation of proposed VGA can be controlled by $\sqrt{\frac{(W/L)_{input}}{(W/L)_{load}}}$ and by $k \propto \frac{I_0}{K}$.

With $|V_{th}| \approx 0.43$ and choosing $\frac{(W/L)_{input}}{(W/L)_{load}} = 50$, the ideal gain vs Vc at different values of k is shown in Figure 2.

This work was achieved in the framework of the Erasmus+ CONN'COR project no. 2024-1-FR01-KA220-HED-000250882 in R3 4"Research-based teaching" in the ICS Master at University Paris Saclay

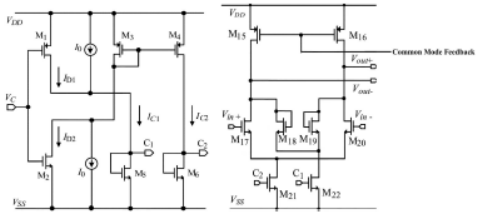

Fig. 1. Schematics of VGA

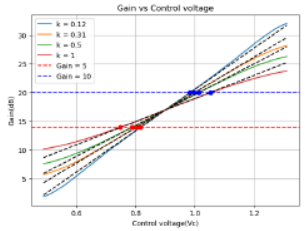

Fig. 2. Gain(dB) vs Vc(V) at different k for $\frac{(W/L)_{input}}{(W/L)_{load}} = 50$

B. Valid range of operation

Each transistor needs to operate in saturation mode so that equation(1) is valid. Therefore, the demension of control stage needs to satisfy Equation(3), and the dimension of amplifying stage needs to satisfy Equation(4).

The output voltage swing may cause one of M18 and M19 locked in cut off mode, as shown in Figure 3. Equation(5) needs to be held to avoid such undesired equilibrium.

Design of a Compact Low Power 10 nF Capacitance Multiplier for Biomedical Applications

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[2]*ICS Master student, Université Paris Saclay,* France
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***Abstract*—In many biomedical circuits, such as notch filters, relaxation oscillators, H-bridge stimulation circuits, and voltage multiplication, large capacitance values are often required. However, integrating such capacitors on-chip presents significant challenges due to the extensive silicon area they occupy. Capacitance multipliers have been proposed to address this issue, though the inclusion of active elements typically results in increased power consumption. To mitigate this, a low-power Gm-based capacitance multipliers, which operates in weak inversion region to minimize the bias current and power consumption, is presented in this paper. The proposed circuit achieves a multiplication factor of 10000, leading to an effective capacitance of 10 nF based on a 1 pF integrated MIM capacitor. Post layout simulation result shows that it operates with very low average power consumption of 56.74 nW and occupies a compact area of 92.545 μm×35 μm, in contrast to the 1 mm² required for a 1 nF capacitor in a 0.18 μm CMOS process.**

***Index Terms*—analog integrated circuits, capacitance multiplier, subthreshold**

I. Introduction

Capacitance multipliers are used to emulate large capacitors instead of employing bulky passive components. However, incorporating active elements in capacitance multipliers increases power consumption. Therefore, optimizing both size and power efficiency is crucial in capacitance multiplier design. There have been many contributions to this topic; however, most studies are not optimized for power consumption. In [1], a current-mode circuit employing a single differential pair is proposed to reduce mismatch effects between the two Operational Transconductance Amplifier (OTA) stages, while current multiplication exponentially increases the multiplication factor. However, the power consumption is relatively high — 1.32 mW — making it unsuitable for low-power applications. In [2], an electrically tunable floating capacitance multiplier is implemented using four Bipolar transistors (BJT) OTAs with a grounded base capacitance. Although this approach can achieve a gain factor as high as 10^6, it does so at the expense of increased bias current, leading to a high power consumption. An effective way to reduce power consumption is to operate the transistors in the weak inversion region, which enables lower voltage operation and reduced power supply requirements. Thanks to the transconductance–current characteristic of Metal-Oxide-Semiconductor Field-Effect (MOSFET) transistors in the weak inversion region, the circuit in [3] employs the translinear principle, allowing for low supply voltage and bias currents. Similarly, [4] presents a capacitance multiplier using subthreshold second generation current conveyor (CCII) and OTA, capable of achieving a very high multiplication gain. However, its power consumption still remains in the microwatt range. Thus, designing a capacitance multiplier with a wide multiplication range and extremely low power consumption remains a significant challenge. The objective of this work is to design a capacitance multiplier that achieves a high multiplication gain while maintaining low power consumption in the range of nanowatts.

This paper will present a four-stage OTA-based capacitance multiplier designed to operate in the subthreshold region. The subthreshold OTA employs a two-stage current mirror to minimize size and ensure the desired output bias.

This work was partially achieved in the framework of the Erasmus+ CONN'COR project no. 2024-1-FR01-KA220-HED-000250882 in R3_4 "Research-based teaching" in the ICS Master at Univerisity Paris Saclay

II. Proposed Architecture

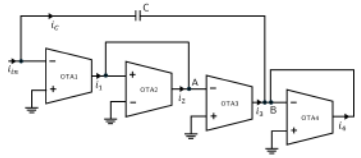

Fig. 1. Schematic of proposed capacitance multiplier.

The proposed architecture, shown in Figure 1, consists of four OTAs. When an AC signal is applied to the negative input terminal of OTA1, the input current is given by $i_{in} = i_C$. The output current of OTA3 can be calculated as:

$$i_3 = -V_A g m_3 = -\frac{V_{in} g m_1 g m_3}{g m_2} \quad (1)$$

Meanwhile, the output current of OTA4 is obtained by:

$$i_4 = -V_B g m_3 = -(V_{in} - i_{in} Z_C) g m_4 \quad (2)$$

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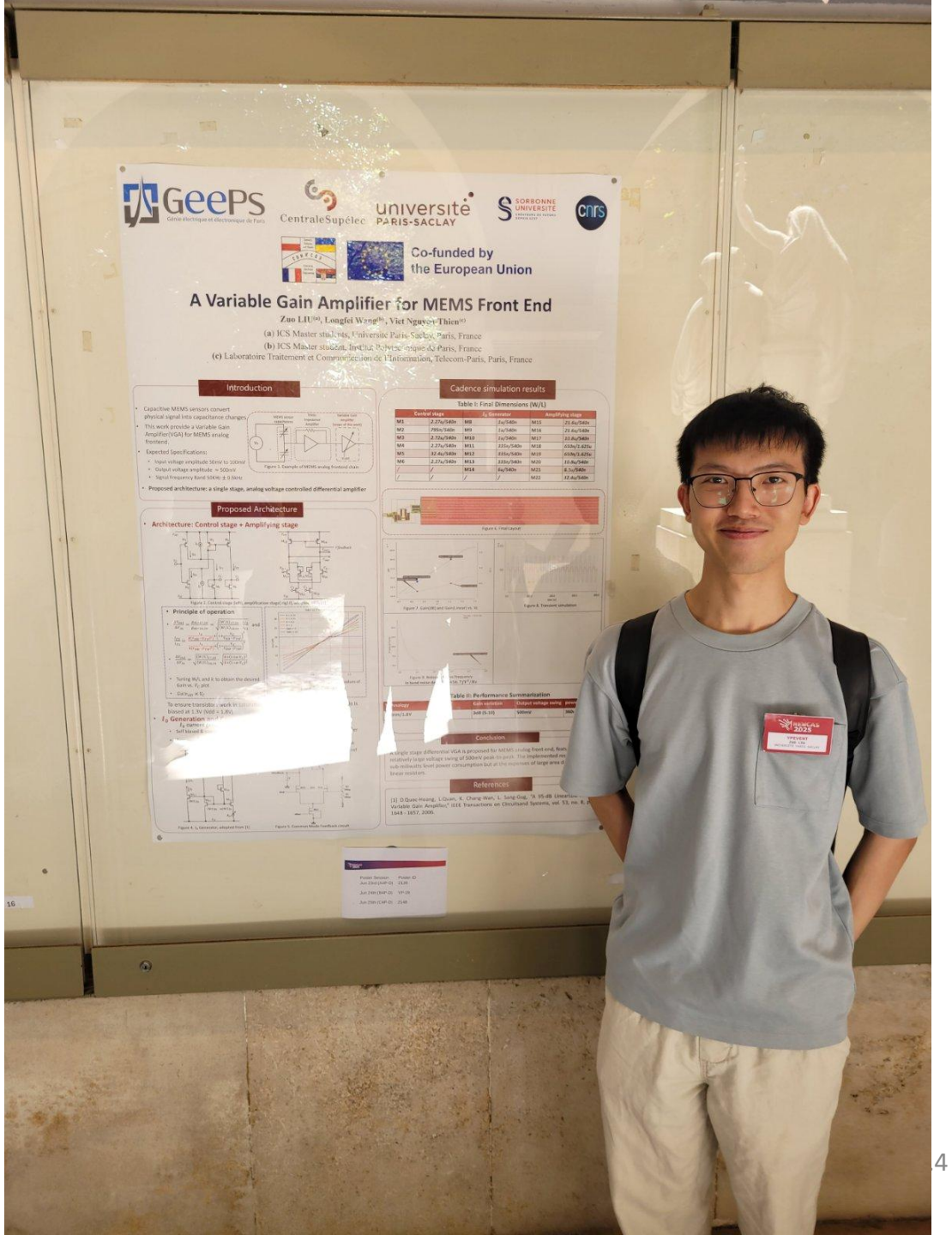
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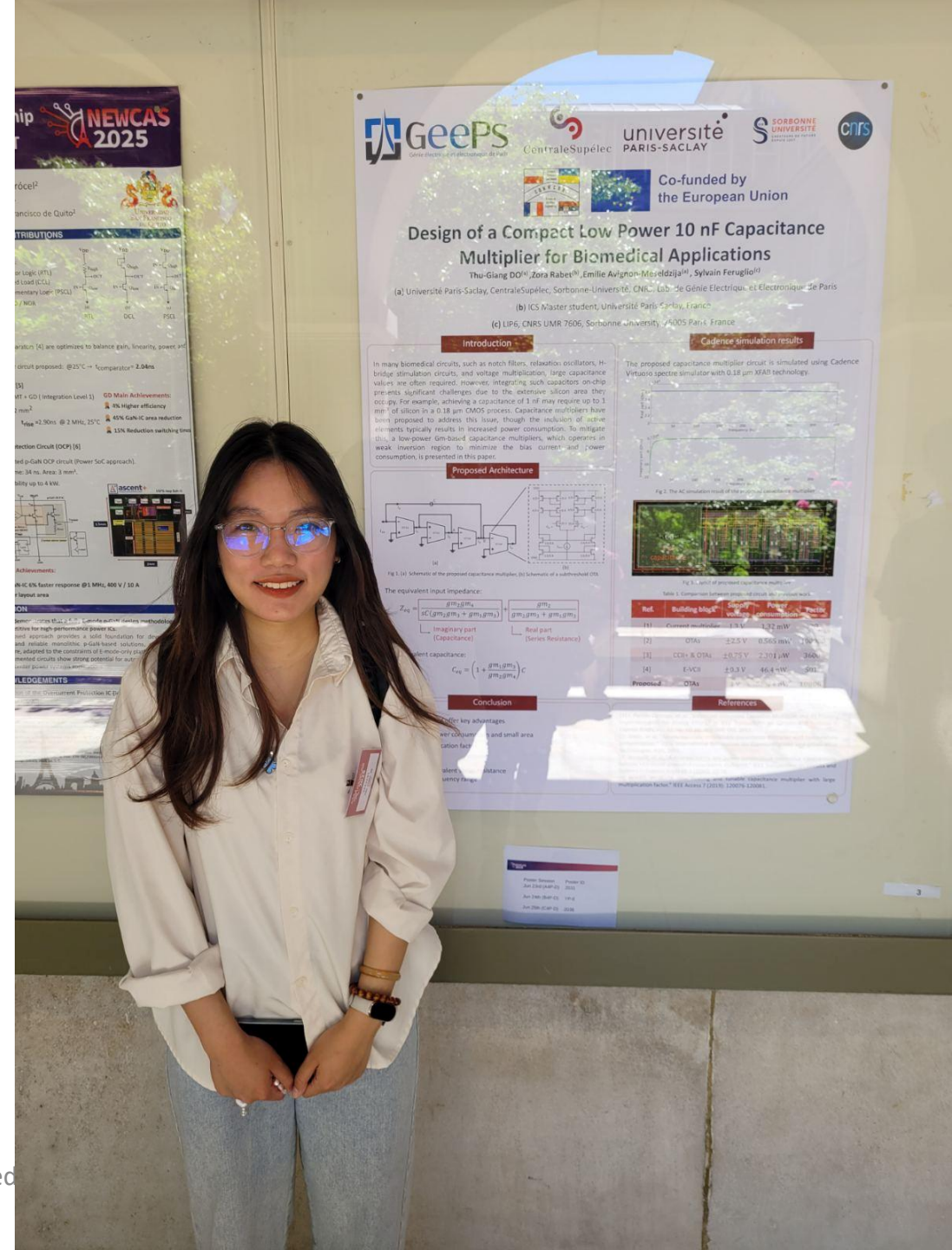
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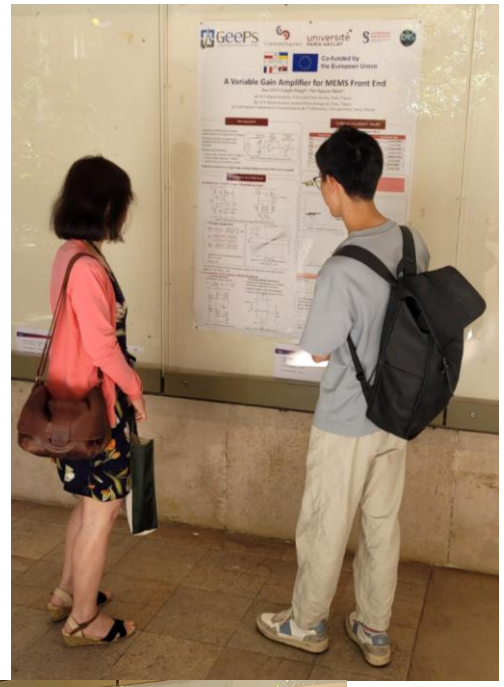
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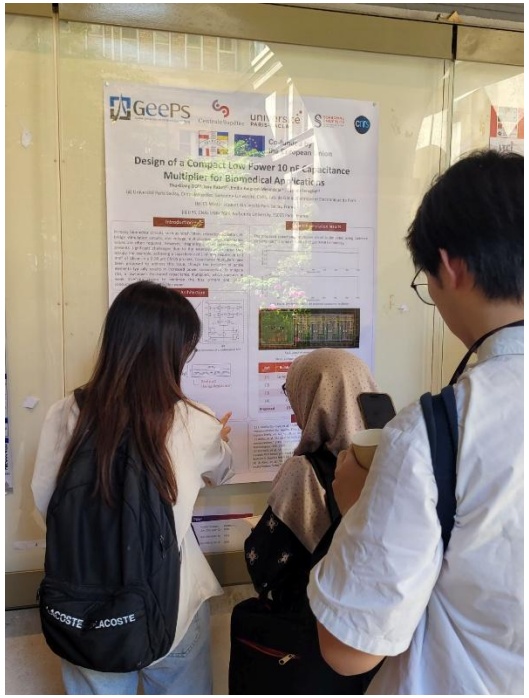
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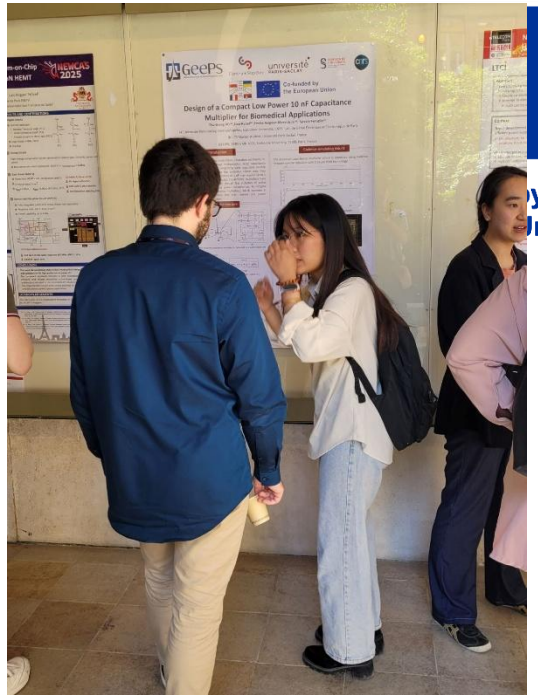
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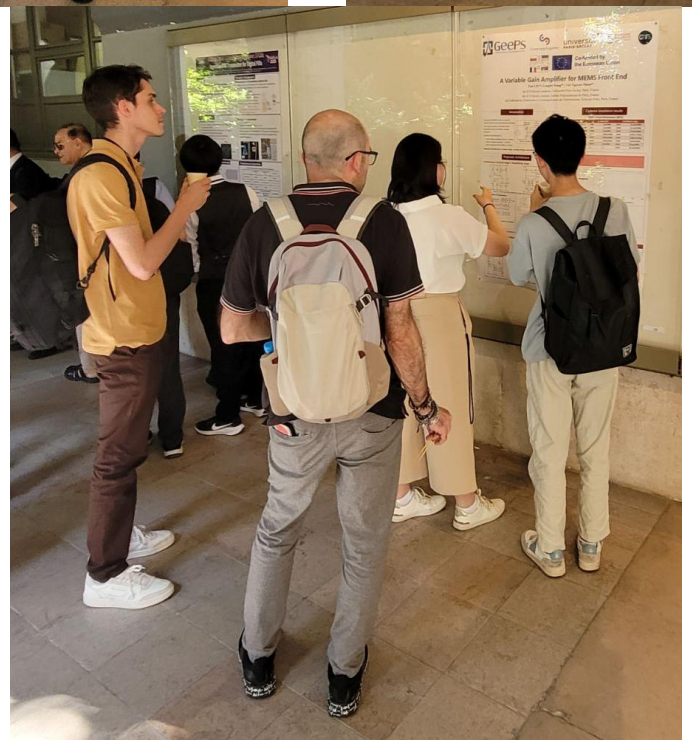
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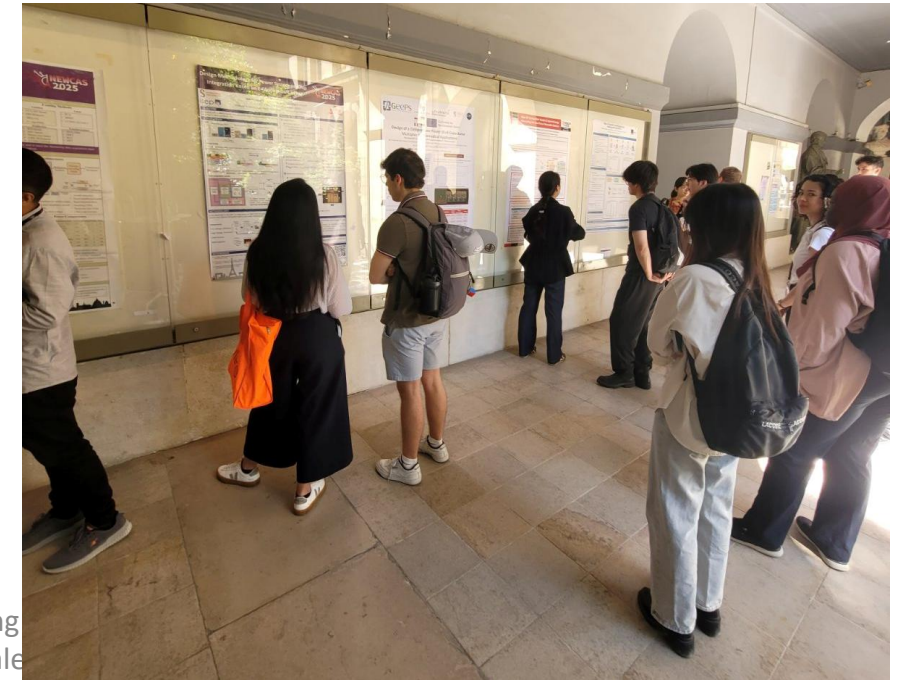

Outline

1. Context and Organization
2. Preparation steps
3. Evaluation of the work
4. Valorization and networking
5. Results of students survey
6. Conclusion

CAD2 "Research Based Teaching"

This form will allow us to get your opinion about this kind of teaching, in the framework of the Erasmus+ project CONN'COR

If you enjoyed this research based teaching, what are the reasons?

- ○ I can work independantely and make my own proposition (subject, architecture, topic...)
- ○ I can learn new aspects of circuit design (noise, subthreshold, new architectures...)
- ○ It gives me an idea of what is research in the field of integrated circuits design
- ○ I plan to continue with a PhD so this is a good introduction
- ○ Autre : _____

If you did not enjoyed this research based teaching what are the reasons?

- ○ Reading the articles related to the subject is really difficult
- ○ We lack time in the proposed format, 24hours is not enough
- ○ I do not want to continue in research so I don't think it is useful
- ○ I prefer to be guided, with all known answers
- ○ I prefer when the subject is the same for all the students
- ○ Autre : _____

Results of students survey

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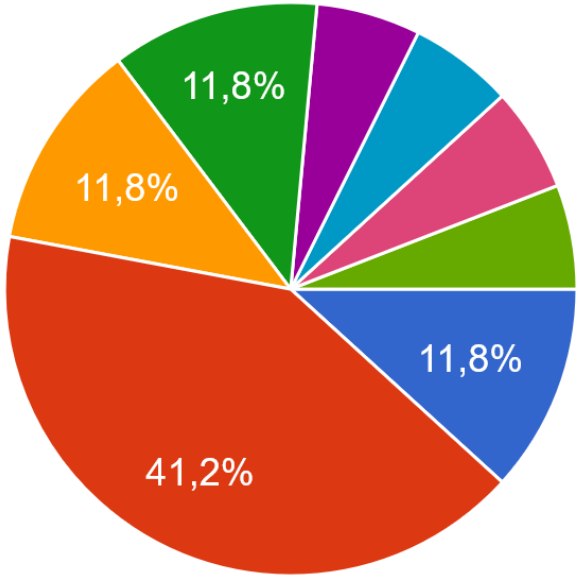
If you enjoyed this research based teaching, what are the reasons?

17 réponses



- I can work independantely and make my own proposition (subject, architecture,…
- I can learn new aspects of circuit design (noise, subthreshold, new architecture…
- It gives me an idea of what is researc…
- I plan to continue with a PhD so this is…
- I can learn new aspects on a subject t…
- All of the above, it is a really interestin…
- All of the 4 answers above
- It was good to explore cutting-edge re…

Results of students survey

If you did not enjoyed this research based teaching what are the reasons?

13 réponses

Conclusions (1)

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Teachers point of view:

Teaching based on research needs a specific and huge preparation:

- Specific pre-selection of research work
- Creation of numerous tutorial
- Specific and individual or pair support between sessions

Conclusions (2)

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Students point of view:

- « Negative feedbacks »:
  - Some subjects more difficult than others
  - Lack of time
  - Want to be guided on a identical subject
- « Positive feedbacks »:
  - They can learn new aspects of circuit design
  - Gives an idea of what is research
  - Can work idependantly and make own proposition
  - Good to explore cutting-edge research/implementations