Design of a Compact Low Power 10 nF Capacitance Multiplier for Biomedical Applications

Thu Giang Do[1], Zohra Rabet[2], Émilie Avignon-Meseldzija[1], Sylvain Feruglio[3]
[1]*Université Paris-Saclay, CentraleSupélec, CNRS, Laboratoire de Génie Electrique et Electronique de Paris, CentraleSupélec,* 91192 Gif-sur-Yvette, France
[2]*ICS Master student, Université Paris Saclay,* France
[3]*LIP6, CNRS UMR 7606, Sorbonne University,* 75005 Paris, France

***Abstract*—In many biomedical circuits, such as notch filters, relaxation oscillators, H-bridge stimulation circuits, and voltage multiplication, large capacitance values are often required. However, integrating such capacitors on-chip presents significant challenges due to the extensive silicon area they occupy. Capacitance multipliers have been proposed to address this issue, though the inclusion of active elements typically results in increased power consumption. To mitigate this, a low-power Gm-based capacitance multipliers, which operates in weak inversion region to minimize the bias current and power consumption, is presented in this paper. The proposed circuit achieves a multiplication factor of 10000, leading to an effective capacitance of 10 nF based on a 1 pF integrated MIM capacitor. Post layout simulation result shows that it operates with very low average power consumption of 56.74 nW and occupies a compact area of 92.545 μm$\times$35 μm, in contrast to the 1 mm² required for a 1 nF capacitor in a 0.18 μm CMOS process.**

***Index Terms*—analog integrated circuits, capacitance multiplier, subthreshold**

I. Introduction

Capacitance multipliers are used to emulate large capacitors instead of employing bulky passive components. However, incorporating active elements in capacitance multipliers increases power consumption. Therefore, optimizing both size and power efficiency is crucial in capacitance multiplier design. There have been many contributions to this topic; however, most studies are not optimized for power consumption. In [1], a current-mode circuit employing a single differential pair is proposed to reduce mismatch effects between the two Operational Transconductance Amplifier (OTA) stages, while current multiplication exponentially increases the multiplication factor. However, the power consumption is relatively high — 1.32 mW — making it unsuitable for low-power applications. In [2], an electrically tunable floating capacitance multiplier is implemented using four Bipolar transistors (BJT) OTAs with a grounded base capacitance. Although this approach can achieve a gain factor as high as 10^6, it does so at the expense of increased bias current, leading to a high power consumption. An effective way to reduce power consumption is to operate the transistors in the weak inversion region, which enables lower voltage operation and reduced power supply requirements. Thanks to the transconductance–current characteristic of Metal-Oxide-Semiconductor Field-Effect (MOSFET) transistors in the weak inversion region, the circuit in [3] employs the translinear principle, allowing for low supply voltage and bias currents. Similarly, [4] presents a capacitance multiplier using subthreshold second generation current conveyor (CCII) and OTA, capable of achieving a very high multiplication gain. However, its power consumption still remains in the microwatt range. Thus, designing a capacitance multiplier with a wide multiplication range and extremely low power consumption remains a significant challenge. The objective of this work is to design a capacitance multiplier that achieves a high multiplication gain while maintaining low power consumption in the range of nanowatts.

This paper will present a four-stage OTA-based capacitance multiplier designed to operate in the subthreshold region. The subthreshold OTA employs a two-stage current mirror to minimize size and ensure the desired output bias.

This work was partially achieved in the framework of the Erasmus+ CONN'COR project no. 2024-1-FR01-KA220-HED-000250882 in R3_4 "Research-based teaching" in the ICS Master at Univerisity Paris Saclay

II. Proposed architecture

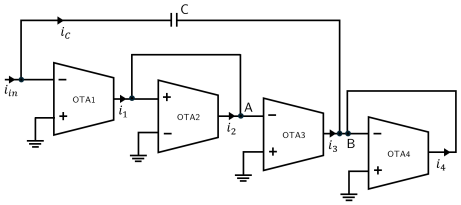

Fig. 1. Schematic of proposed capacitance multiplier.

The proposed architecture, shown in Figure 1, consists of four OTAs. When an AC signal is applied to the negative input terminal of OTA1, the input current is given by $i_{in} = i_C$. The output current of OTA3 can be calculated as:

$$i_3 = -V_A g m_3 = -\frac{V_{in} g m_1 g m_3}{g m_2} \tag{1}$$

Meanwhile, the output current of OTA4 is obtained by:

$$i_4 = -V_B g m_3 = -(V_{in} - i_{in} Z_C) g m_4 \tag{2}$$

According to KCL, we have:

$$i_{in} = -i_3 - i_4 = \frac{V_{in} gm_1 gm_3}{gm_2} + (V_{in} - i_{in} Z_C) gm_4 \quad (3)$$

which can be rewritten as

$$i_{in}(1 + gm_4 Z_C) = V_{in} \left(\frac{gm_1 gm_3}{gm_2} + gm_4 \right) \quad (4)$$

From Equation 4, the equivalent input impedance will be:

$$Z_{eq} = \frac{gm_2 gm_4}{sC(gm_2 gm_4 + gm_1 gm_3)} + \frac{gm_2}{gm_2 gm_4 + gm_1 gm_3} \quad (5)$$

This impedance can be decomposed into two components: a real part, representing an equivalent series resistance (ESR) and an imaginary part, corresponding to an equivalent capacitance, as expressed below:

$$R_{eq} = \frac{gm_2}{gm_2 gm_4 + gm_1 gm_3} \quad (6)$$

and

$$C_{eq} = \left(1 + \frac{gm_1 gm_3}{gm_2 gm_4} \right) C \quad (7)$$

By adjusting the ratio of gm_1 and gm_3 to be significantly larger than that of gm_2 and gm_4, a large effective capacitance can be achieved while maintaining a small ESR. The OTA architecture used in this work is based on the design in [4], which is optimized for subthreshold operation. In this weak inversion region, the transconductance gm primarily depends on the bias current I_{bias}.

III. Simulation Results

The proposed capacitance multiplier circuit is simulated using Cadence Virtuoso spectre simulator with $0.18\,\mu$m XFAB technology. The transconductance values of OTA1 to OTA4 are adjusted through the bias currents I_{bias1} to I_{bias4}. In this design, we set $I_{\text{bias1}} = I_{\text{bias3}} = 16\,\text{nA}$ and $I_{\text{bias2}} = I_{\text{bias4}} = 0.16\,\text{nA}$. The bias input voltages of each OTA are carefully designed to ensure stable operation around the intended bias point of 300 mV.

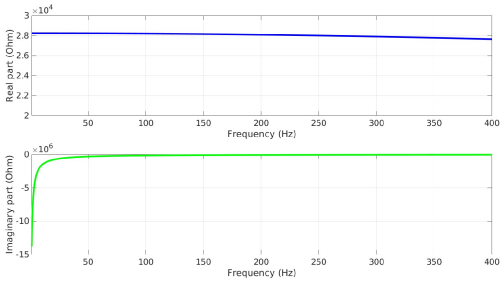

Fig. 2. AC simultion result of the proposed capacitance multiplier.

To verify the design, we plot the simulated real and imaginary parts of the input impedance as shown in Figure 2. As observed from the results, the real part is only a few tens of kΩ, while the imaginary part approaches zero as frequency increases, confirming that the imaginary component is capacitive. The circuit achieves an equivalent capacitance of 10 nF from a 1 pF capacitor. It operates effectively over the frequency range of 1 to 400 Hz to ensure a maximum error of 0.8 nF (8%). The power consumption recorded by the simulator is 58.45 nW for a total multiplication gain of 10000.

The comparison between the performance of proposed capacitance multiplier and previous works can be summarized as in Table 1. The proposed circuit significantly reduces power consumption compared to other works while maintaining a high capacitance factor.

TABLE I
Comparison between proposed circuit and previous works

Ref.	Building Block	Supply Voltage	Power consumption	Factor
[1]	Current multiplication	1.3 V	1.32 mW	28
[2]	OTAs	±2.5 V	0.565 mW	100000
[3]	CCII+ & OTAs	±0.75 V	2.301 μW	3600
[4]	E-VCII	±0.3 V	46.4 nW	561
This work	OTAs	1 V	56.74 nW	10000

The layout of the capacitor multiplier (Figure 3) occupies an area of approximately $92.545\mu\text{m}\times35\mu\text{m}$.

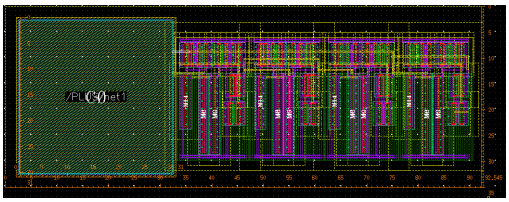

Fig. 3. Layout of the proposed capacitance multiplier.

IV. Conclusion

In this paper, a low-power, low-area capacitance multiplication circuit based on G_m has been proposed. For a very high multiplication factor of 10000, the circuit consumes only 56.74 nW, which is significantly lower than other designs. The proposed design offers key advantages including ultra-low power consumption, high accuracy, a large multiplication factor, and a compact silicon area. In the future, this work can be extended to reduce ESR and enhance the frequency range.

References

[1] I. Padilla-Cantoya, et al. "Enhanced Grounded Capacitor Multiplier and Its Floating Implementation for Analog Filters," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 10, pp. 962-966, Oct. 2015, doi: 10.1109/TCSII.2015.2435751.

[2] Jaikla,, et al. "An electronically controllable capacitance multiplier with temperature compensation." 2006 International Symposium on Communications and Information Technologies. IEEE, 2006.

[3] Stornelli, et al. "A new extremely low power temperature insensitive electronically tunable VCII-based grounded capacitance multiplier." IEEE Transactions on Circuits and Systems II: Express Briefs 68.1 (2020): 72-76.

[4] Al-Absi, et al. "A new floating and tunable capacitance multiplier with large multiplication factor." IEEE Access 7 (2019): 120076-120081.